A SYSTEM FOR TESTING MULTIPLE PARAMETERS OF ACTIVE APERTURE ANTENNA SUBARRAYS

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Abstract

When a phased array antenna consists of a number of complex subarrays, efficient and accurate testing of the subarrays is essential for overall project success. This paper presents a flexible system for testing various parameters of a subarray of an active aperture phased array antenna including S-parameters, noise figure, spurs, oscillations, and peak and average power. Testing is done for both CW and a variety of pulsed signals. A system block diagram is presented and system architecture explained. Timing diagrams are included for testing multiple states (which correspond to antenna beams), channels, and frequencies. Measured verification results are presented.

Keywords: **Component Measurements, Phased Arrays**

1.0 Introduction

This paper describes a multi-purpose measurement system for testing subassemblies of phased array antennas. The system includes appropriate instrumentation to measure the following parameters:

- S-Parameters (Pulsed or CW)
- Peak Power (Pulsed or CW)
- Average Power (Pulsed or CW)
- Noise Figure
- Spurs and Oscillations

The system also includes control of various state machine parameters in the Device Under Test (DUT) and handshaking ability with the DUT for the change of those states.

2.0 Test System Requirements

This system was designed to test a single element or a subset of the complete beam forming network feeding a phased array antenna. Such networks typically include amplifiers, phase shifters, couplers, and power dividers/combiners. For this system the DUT as configured for test had 4 interface ports. Specific test requirements are listed in Table 1.

Parameter	**Requirement**
S-Parameter Measurements	
Port 1 to Port 4	2 to 12 GHz
Port 2 to Port 4	8 to 12 GHz
Port 3 to Port 4	8 to 12 GHz
Measurement Speed	10,000 / sec
RF Drive Levels	
Port 1	+15 dBm
Port 2	+ 7 dBm
Port 3	+ 7 dBm
Port 4	+13 dBm
Maximum Input Power	
Port 1	+15 dBm
Port 2	+27 dBm
Port 3	+25 dBm
Port 4	+34 dBm
Dynamic Range	> 65 dB
Pulse Measurement Capability	
Duty Cycle	<1% to CW
Pulse Width	100 nsec, min
PRF	1 MHz, max
Pulse Rise/Fall Time	<10 nsec
Peak Power (Pulsed or CW) Port 1 to Port 4	.3 dB accuracy
Average Power (Pulsed or CW) Port 1 to Port 4	.3 dB accuracy
Noise Figure Measurement Port 2 to Port 4, Port 3 to Port 4	.5 dB accuracy

Table 1. Test System Requirements

3.0 System Description and Block Diagram

As noted above the system includes all of the instrumentation to perform a number of different types of measurements on the DUT. A block diagram of the system is shown in Figure 1.

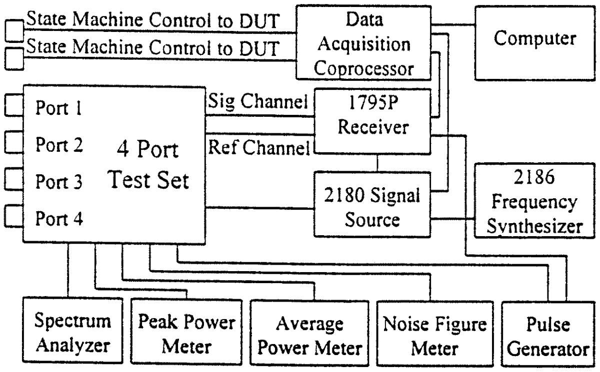

Figure 1. System Block Diagram

The system controller (computer), in conjunction with the Data Acquisition Coprocessor (DAC), controls the command and data flow to the measurement instruments over the GPIB and high speed parallel interface. The DAC is resident on the CPU bus and consists of a DSP microprocessor which controls the data collection task. The DAC provides direct hardware control of the data acquisition process by issuing triggers to and receiving triggers from the measurement receiver, signal source, test set, and state machine control. Data is captured in rotating buffers for eventual transfer to the system controller. This high-speed interface is essential to increase system speed since exclusive use of the GPIB would dramatically increase test time.

The distributed instrument control methods require only 15% of the system CPU's time during full speed data collection activities. The remaining 85% is available for real-time vector error correction or data analysis. Real-time error correction is accomplished by utilizing the multitasking capabilities of the OS/2® operating system, with the CPU's internal numeric coprocessor applying the error correction algorithm "on-the-fly." The GPIB is used only for instrument initialization and error monitoring.

4.0 RF Test Set

The heart of the system is the 4 Port RF Test Set and the Scientific-Atlanta Model 1795P Microwave Receiver. The test set includes switches for configuring the system for the various tests, couplers for providing appropriate reference signals, amplifiers for boosting the RF signal, and step attenuators to provide power leveling.

The portion of the test set used for S-parameter measurements is a fully automatic reversing test set designed specifically for high-speed measurements. It utilizes high-speed, fast-settling PIN diode switches that operate synchronously with the measurement cycle. These switches have 110 dB isolation between ports which reduces crosstalk terms to negligible levels.

DUT excitation is connected to the RF IN port of the test set. A broadband coupler provides a sample of the excitation signal for the reference channel mixer which provides the phaser reference for the system. A high speed switch sets the direction for forward or reverse measurements. A bias "T" is provided on each port to facilitate active device characterizations without special fixturing. Broadband, high-directivity couplers are used to separate the incident and reflected waves present at the test ports. A unique feature of this test set architecture is the use of two couplers at each port. This design permits the incident power to be sampled near the test port rather than using the signal from the reference coupler port while retaining the high directivity required for precision measurements. The signals from the couplers are then switched appropriately into the test channel to measure the desired S-parameter. The system software includes capability for making raw S-parameter measurements or applying normalization or 3, 8 or 12 term error correction.

Since many subassemblies of phased arrays are non-linear devices, performing tests with level input power becomes important. Prior to performing S-parameter, power, or spur measurements the user performs a power calibration. During a power calibration the power sensor is connected to the appropriate port interface where the DUT will the connected. At each frequency the power is measured and step attenuators are adjusted within the test set until the desired power level is reached. The step attenuators have a resolution of 0.015 dB so that a power level may be calibrated to within 0.02 dB. The values of the step attenuators are then stored in a table and are output by the DAC on a frequency-by-frequency basis to the test set during the actual measurement process to insure a stable power level. With a controlled temperature environment, a power calibration can hold the output power of the test set to within 0.1 dB of the desired level over a very long time period.

Measurement accuracies of peak and average power, noise figure, spurs, and oscillations are limited by the measurement accuracy of the specific instruments used for the measurement. For these measurements the system must account for the loss of the test set between the DUT and the instrument. Losses are measured and entered into calibration tables and are applied real time to the appropriate measurements.

5.0 Pulse Measurement Capability

Since many phased array antennas transmit very high power, requirements often exist to test the DUT in a pulse mode with high input power. This system utilizes a pulse generator to modulate the RF input signal to the DUT and synchronize the measurement made by the 1795P Receiver.

The 1795P Receiver uses a local oscillator for conversion of the RF signal to a 45 MHz IF. The 1795P Receiver then directly digitizes this IF and performs all subsequent processing in the digital domain. The 1795P Receiver provides greater dynamic range than previous pulsed receivers by maintaining the wide IF bandwidth required for short pulse detection.

6.0 System Timing and State Machine Control

State machines of the DUT are controlled via five 16 bit words issued from the system. Thus each of the state machines may have a maximum of 65,535 states ranging from 0000 to FFFE. The RF measurement can be made versus state which can be specified as a single value, range, or a list. The user may program an optional trigger to be issued to the DUT at the point of change of the state machines. He may also select an option of waiting for a DUT ready signal before beginning the measurement. A timing diagram of the measurement sequence is shown in Figure 2.

In this diagram it is assumed the user has selected the trigger and DUT ready signal options. At the beginning of the measurement. Approximately 5.5 µsec into the receiver idle period the representative state machine bit is set to the desired level. After an additional 2.5 µsec delay to insure the state machine bit is at the appropriate level, the trigger is issued to the DUT. The length of the trigger is user programmable. In the particular device tested by this system, the DUT ready signal goes low when it receives the trigger signal. The system monitors the DUT ready line and will not perform any measurements while it is low. Once the DUT has implemented all of the appropriate states as commanded by the state machine bits, it sends the DUT ready signal high. At this point the 1795P Receiver begins making its measurement.

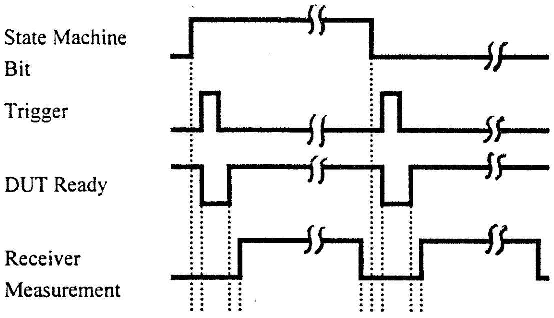

Figure 2. Timing Diagram with Trigger and Ready Signal

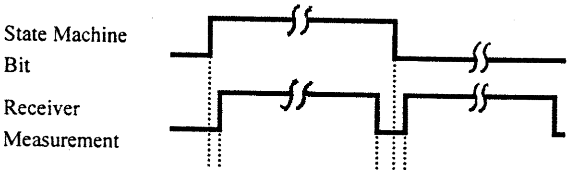

Figure 3. Simplified Timing Diagram

Figure 3 shows a simplified timing diagram for a case where trigger and DUT ready signals are not enabled. For this case the total measurement time is 8 µsec for the state machine change plus receiver measurement time (determined by number of channels and averages).

Speed of the test system was a major concern since a typical test scenario involved measuring 4 S-parameters for 2 state machines with 64 states each for 41 frequencies (8 to 12 GHz every 100 MHz) for a total of over 1 million receiver channel measurements. A receiver setting of 4 averages was chosen to achieve a minimum dynamic range of 80 dB (based on measured dynamic range of 75 dB minimum for 1 average). Note for the following calculations that measurement of 4 S-parameters actually requires the measurement of 6 receiver channels because of the required ratios.

Measurement time for this measurement is as follows:

4,096 States * [4 S-parameters (6 channels) * 400 µsec (for 4 averages) + 8 µsec to change states] = 9.863 sec/frequency

Time to Change Frequency = 10 msec + 25µsec/MHz step

Total measurement time = 41 Freq * 9.863 sec/freq + 40 Freq Changes * 12.5 msec = **404.9 sec = 6.7 minutes**

Parameter	Time (sec)	Percent
Receiver Measurement Time	403.05	99.6%
Time to Change States	1.34	0.3%
Time to Change Frequency	0.50	0.1%
Total	404.89	100.0%

Table 2. Summary of Typical Measurement Time

As Table 2 shows, the total measurement time is dominated by the receiver measurement time. You can see that a reduction in test speed even by a factor of 2 would have serious impacts on overall system test time.

7.0 Verification Results

7.1 Power Output

Figure 4 shows the measured power output from Port 1 after calibrating for +15 dBm power output. Note the maximum variation from the specified output power is less than 0.1 dB.

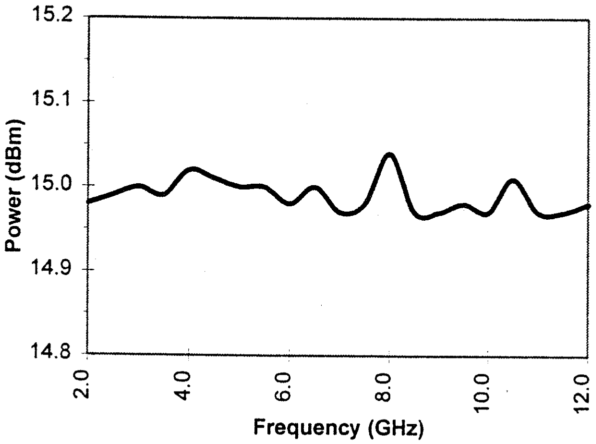

Figure 4. Measured Output Power from Port 1 after Power Calibration

7.2 S-Parameter Measurement Accuracy

Figures 5 and 6 show amplitude and phase measurements of a 50 dB calibrated attenuator in both CW and pulsed modes as well as the calibration values. The pulsed measurements were made with a pulse width of 35 µsec and a pulse repetition rate of 10 kHz (for a 35% duty cycle). The attenuator calibration accuracy was ±0.18 dB in amplitude and ±4.6 degrees in phase. Table 3 shows the statistical agreement of the measurements. Note that almost all measurements were within the calibration accuracy of the attenuator. (Receiver accuracy is a function of the level below compression, so measurement of a 50 dB attenuator is a rigorous test. Measurements on a device with less loss would be even more accurate.)

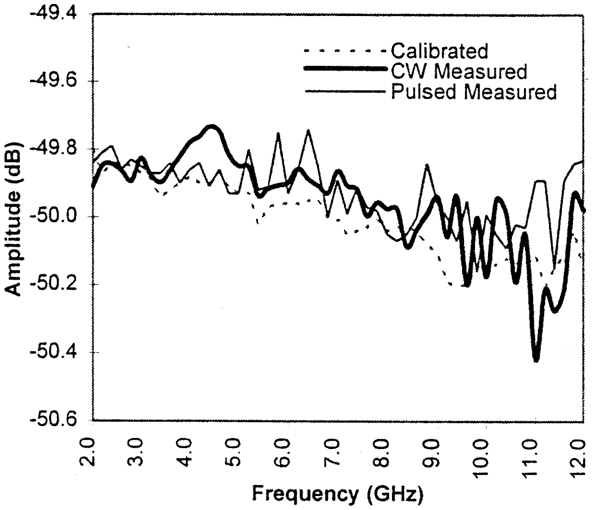

Figure 5. Comparison of Measured Attenuator Value to Calibrated Attenuator Value

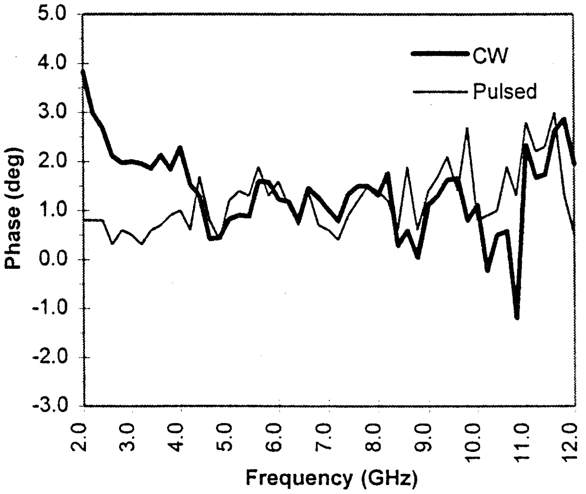

Figure 6. Difference Between Measured and Calibrated Phase of Attenuator

Parameter	Peak Deviation	Average Deviation
CW Amplitude	.31 dB	.07 dB
Pulsed Amplitude	.32 dB	.08 dB
CW Phase	3.8 deg	0.6 deg
Pulsed Phase	3.0 deg	0.5 deg

Table 3. Statistical Agreement of Measured versus Calibrated Attenuator Values

7.3 Dynamic Range

Figure 7 shows the dynamic range for a single average for an S-parameter measurement made between Port 1 and Port 4. The miminimum dynamic range was 77 dB. Significant increases in dynamic range can be obtained by increasing the number of averages of the 1795P Receiver.

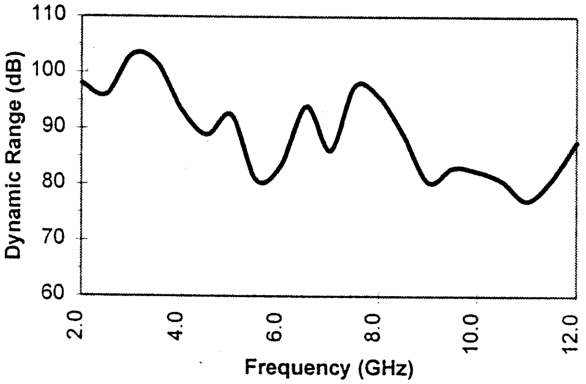

Figure 7. Dynamic Range

8.0 Summary

This paper has presented a versatile system for testing RF components used in phased array antennas. Such antennas often have high output power and heat dissipation issues which require them to be tested in the pulsed configuration in which they will be operated. The high speed system can perform a variety of tests providing complete and accurate characterization of the DUT for both pulsed and CW operation. By providing the user control over many test variables including DUT input power and monitoring of DUT ready signals, the user can be assured of the validity of the results.

Verification results for S-parameters show excellent agreement with calibrated standards. The system provides a minimum of 77 dB dynamic range which can be increased by increasing the number of averages used in receiver measurements. Accuracy of noise figure, power, and spectrum analyzer measurements are limited only by the accuracies of the chosen instrumentation.

Use of this test system can significantly reduce the time required for testing the beam forming network of a phased array antenna. By providing the user access to accurate measurements in a fully integrated system, overall DUT testing is greatly simplified.